

REMARKS

Claims 45-60, 62-77, and 79-84 remain in this application. Claims 61 and 78 have been cancelled without prejudice. Claims 45, 50, 63, and 74 have been amended. The amendments are supported by the specification and no new matter has been added. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

Drawings

The Examiner has objected to the drawings under 37 CFR 1.83(a). The Applicants have amended claim 45 to remove the recitation of the fourth signal interconnect line. The Applicants have cancelled claims 61 and 78 without prejudice. The Applicants reserve the right to re-introduce these claims at a later date along with new or amended drawings showing the third plurality of conductive lines having the third dielectric therebetween. Additionally, the Applicants enclose herewith formal drawings as required by the Examiner.

35 U.S.C. §103(a) Rejection – Usami in view of Havemann and Doo

The Examiner has rejected claims 45-49 and 63-73 under 35 U.S.C. §103 (a) as being unpatentable over U.S. Patent No. 6,222,269 to Usami (hereinafter referred to as “Usami”) in view of U.S. Patent No. 5,751,066 to Havemann (hereinafter “Havemann”) and U.S. Patent No. 4,153,988 to Doo (hereinafter “Doo”).

Claim 45 recites at least, *“patterning the mask layer such that the first and second power interconnect lines and a first portion of the patterned first layer are covered, and the third signal interconnect line and a second portion of the patterned first layer are uncovered”* and *“depositing a second layer of a second dielectric material adjacent to the third signal interconnect line between the second power interconnect line and the third signal interconnect*

line, the second dielectric material having a smaller dielectric constant than the first dielectric material”.

Usami and Havemann do not teach or suggest: (1) power lines, (2) patterning such that power lines are covered and a signal line is uncovered, nor (3) depositing a smaller dielectric constant material between signal lines than between a power line and a signal line.

The Examiner has admitted that Usami lacks specifying that the plurality of interconnect lines include power interconnect lines (first and second) and signal interconnect lines (third and fourth). The Applicants respectfully agree. There is absolutely no mention of power lines in Usami. Furthermore, there is absolutely no mention of power lines in Havemann. Usami and Havemann simply do not discuss power lines or power driver noise. Instead, Usami and Havemann are limited to signal lines. There is absolutely no mention whatsoever that the disclosure has relevance to power lines or power driver noise. This being the case, it is not surprising that there is also no teaching or suggestion of patterning such that power lines are covered and signal lines are uncovered. There is also no teaching or suggestion of depositing a smaller dielectric constant material between a signal line and a power line adjacent to the signal line than between power lines. Accordingly, Usami and Havemann clearly do not teach or suggest the limitations of claim 45.

The Examiner has proposed modifying Usami based on Doo in order to reject claim 45. The Examiner has stated that Doo teaches that increasing the capacitance of a power line will reduce driver noise. The Examiner has further stated that:

“Anyone in the semiconductor art would realize that, for a given separation between a pair of interconnect lines, the capacitance between the pair can be readily increased by utilizing a high-dielectric-constant material between the pair of lines, i.e., can be readily increased in comparison to utilizing a low-dielectric-constant material between the pair of lines. In other words, given (i) a plurality of interconnect lines formed on the same

level of metallization and (ii) two different dielectric-constant materials that are to be incorporated between the plurality of lines, the knowledge generally available to one of ordinary skill in the art clearly shows it is desirable to utilize the lower-dielectric-constant material between the interconnect lines which will be used for signal lines and to utilize the higher-dielectric-constant material between interconnect lines which will be used for power lines.”

The Applicants respectfully disagree with the modification of Usami and/or Havemann and with the obviousness rejection because there is no teaching, suggestion or motivation to modify the references as proposed by the Examiner. To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some teaching, suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. In re Vaack, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The modification proposed by the Examiner is allegedly based on what is known by one of ordinary level of skill in the art. However, it is not known to reduce driver noise between power lines and reduce parasitic capacitance between signal lines in a given interconnect level by using different materials between the power lines than between the signal lines. The Examiner has not documented that this knowledge is available to one of ordinary level of skill in the art. Doo does not discuss using different materials between signal lines and power lines. Usami and Havemann do not discuss power lines or driver noise. Accordingly, the Examiner has not established a prior art teaching, suggestion, or motivation that it would be desirable to use a first dielectric material between a plurality of power lines and a second dielectric material between a

plurality of signal lines. As was stated in *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984), "The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." (emphasis added). Therefore, it is simply improper to add to either Usami or Havemann features for which they have no interest or need, since they do not discuss power lines or power driver noise.

The Examiner's conclusion appears to be based on hindsight reasoning. Only using 20-20 hindsight, with the Applicant's own disclosure serving as a guide or roadmap, would the Examiner concluded that different materials may be used between power lines than between a power line and a signal line to reduce power line driver noise and signal line parasitic capacitance. Certainly this is not taught or suggested in any of the cited art references taken alone or in combination.

Accordingly, claim 45 is believed to be allowable. **Claims 46-49** depend from claim 45 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 63 is believed to be allowable for reasons similar to those discussed above for claim 45. **Claims 64-68** depend from claim 63 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 69 is believed to be allowable for reasons similar to those discussed above for claim 45. **Claims 70-73** depend from claim 69 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

35 U.S.C. §103(a) Rejection – Havemann in view of Doo

The Examiner has rejected claims 50-62 and 74-84 under 35 U.S.C. §103 (a) as being unpatentable over U.S. Patent No. 5,751,066 issued to Havemann (hereinafter referred to as "Havemann") in view of U.S. Patent No. 4,153,988 issued to Doo (hereinafter referred to as "Doo").

Claim 50 is believed to be allowable for reasons similar to those discussed above for claim 45. **Claims 51-55** depend from claim 50 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 56 is believed to be allowable for reasons similar to those discussed above for claim 45. **Claims 57-60 and 62** depend from claim 56 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Claim 74 is believed to be allowable for reasons similar to those discussed above for claim 45. **Claims 75-77 and 79-84** depend from claim 74 and are believed to be allowable therefor as well as for the recitations independently set forth therein.

Conclusion

Applicants respectfully submit that the rejections have been overcome by the amendment and remark, and that the claims as amended are now in condition for allowance. Accordingly, the Applicants respectfully request the rejections be withdrawn and the claims as amended be allowed. The Examiner is requested to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims:

45. (Amended) A method of forming an interconnect structure, comprising:
- forming a first layer of a first dielectric material on a substrate;
- patterning the first layer;
- depositing conductive material over the patterned first layer;
- planarizing the conductive material such that a plurality of interconnect lines are formed including a first and a second power interconnect lines and a third [and fourth] signal interconnect [lines] line;
- forming a mask layer over the plurality of interconnect lines and patterned first layer;
- patterning the mask layer such that the first and second power interconnect lines and a first portion of the patterned first layer are covered, and the third [and fourth] signal interconnect [lines] line and a second portion of the patterned first layer are uncovered;
- removing the second portion of the patterned dielectric material of the first layer from the uncovered portion;
- removing the patterned mask layer; and
- depositing a second layer of a second dielectric material adjacent to the third signal interconnect line between the second power interconnect line and the third [and fourth] signal interconnect [lines] line, the second dielectric material having a smaller dielectric constant than the first dielectric material.

Claims 46 – 49 remain unchanged.

50. (Amended) A method of forming an interconnect structure, comprising:

forming a first layer of a conductive material on a substrate;

forming a first pair of power interconnect lines to distribute power and a second pair of signal interconnect lines to carry signals from the conductive material;

depositing a first dielectric material over and between the first pair and the second pair;

forming a mask layer over the first pair and the second pair and first dielectric material;

patterning the mask layer such that one portion of the dielectric material between one pair is covered and another portion of the dielectric material between another pair is uncovered;

removing the portion of the dielectric material that is uncovered;

removing the patterned mask layer; and

depositing a second dielectric material having a different dielectric constant than a dielectric constant of the first dielectric material where the portion of the dielectric material was removed.

Claims 51 – 60 remain unchanged.

Claim 61 has been cancelled.

Claim 62 remains unchanged.

63. (Amended) A method of forming an interconnect structure, comprising:

forming on a substrate a first intralayer dielectric and a first plurality of signal interconnect lines disposed within the first intralayer dielectric [forming, on a substrate, a first plurality of signal interconnect lines and a first intralayer dielectric disposed between the first plurality of signal interconnect lines];

removing a portion of the first intralayer dielectric;

forming a second intralayer dielectric on the substrate where the first intralayer dielectric was removed; and

forming a second plurality of power interconnect lines in the second intralayer dielectric.

Claims 64 – 73 remain unchanged.

74. (Amended) A method comprising:

providing a substrate; and

making on the substrate an interconnect structure [comprising] containing a first pair of interconnect lines to distribute power having a first dielectric material disposed therebetween and a second pair of interconnect lines to carry signals having a second dielectric material disposed therebetween, wherein the first dielectric material has a first dielectric constant that is greater than a second dielectric constant of the second material.

Claims 75 – 77 remain unchanged.

Claim 78 has been cancelled.

Claims 79 – 84 remain unchanged.